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Effect of Oxygen, Moisture and Illumination on the Stability and Reliability of Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) OTFTs during Operation and Storage

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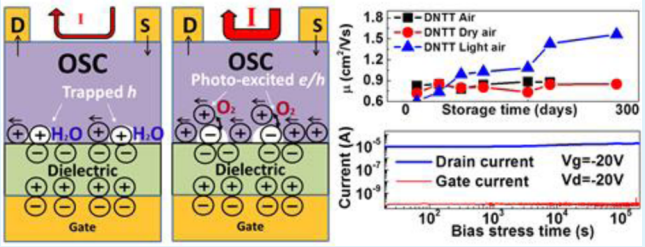
ABSTRACT: We report a systemic study of the stability of organic thin film transistors (OTFTs) both in storage and under operation. Apart from a thin polystyrene buffer layer spin-coated onto the gate dielectric, the constituent parts of the OTFTs were all prepared by vacuum evaporation. The OTFTs are based on the semiconducting small molecule dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) deposited onto the surface of a polystyrene-buffered in situ polymerized diacrylate gate insulator. Over a period of 9 months, no degradation of the hole mobility occurred in devices stored either in the dark in dry air or in uncontrolled air and normal laboratory fluorescent lighting conditions. In the latter case, rather than decreasing, the mobility actually increased almost 2-fold to 1.5 $cm^2/(V{\cdot}s)$. The devices also showed good stability during repeat on/off cycles in the dark in dry air. Exposure to oxygen and light during the on/off cycles led to a positive shift of the transfer curves due to electron trapping when the DNTT was biased into depletion by the application of positive gate voltage. When operated in accumulation, negative gate voltage under the same conditions, the transfer curves were stable. When voltage cycling in moist air in the dark, the transfer curves shifted to negative voltages, thought to be due to the generation of hole traps either in the semiconductor or its interface with the dielectric layer. When subjected to gate bias stress in dry air in the dark for at least 144 h, the device characteristics remained stable.



KEYWORDS: *DNTT, environmental stability, bias stress, OTFTs*

1. INTRODUCTION

Organic thin-film transistors (OTFTs) have been under development for more than two decades,[1] but often show poor environmental stability. For example, OTFTs based upon pentacene and its derivatives show substantial changes in performance during operation in air under ambient conditions.[2−5] Materials such as 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) are becoming popular replacements for pentacene in electronic devices.[6,7] However, these derivatives are themselves still prone to photochemical degradation during processing, which potentially perturbs both the optical absorption and electronic properties of films cast from solution. Upon UV irradiation (~300 nm), TIPS-pentacene forms dimers by cycloaddition[8] and at visible wavelengths is known to photodegrade in solution via a process involving dissolved oxygen.[9,10] The predominant mechanism for this molecule involves activation of O_2 molecules by the initially formed exited state; this either generates singlet O_2 species or superoxide O_2^-, which then adds back across appropriate carbon centers in TIPS-pentacene to produce an endoperoxide (EPO), which is seen as the main product by NMR.[9] By raising the ionization potential of the semiconductor, enhanced environmental stability is inferred, as reported for dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT).[5,11,12] Such a semiconductor or its derivatives could be the key, therefore, to creating opportunities for the general application of OTFTs, including flexible displays, flexible logic and memory devices as well as in sensors. Other materials such as diF-TEST ADT, blends and copolymers are also attracting interest for their high mobility, but little work has yet been reported on the long-term stability of TFTs utilizing them.[13,14] Before exploring possible OTFT applications, it is crucially important to obtain a detailed understanding of the performance and degradation behavior of DNTT OTFTs under different storage and operational conditions. We have already shown that our protocols for fabricating pentacene transistors on a polystyrene (PS)-buffered, flash-evaporated and in situ polymerized tripropylene glycol diacrylate (TPGDA) gate dielectric[15,16] can be used to produce high mobility DNTT transistors ($\mu \sim 1$ $cm^2/(V{\cdot}s)$)[11,12] at high yield from which a

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range of circuits, including ring oscillators and logic gates, can be manufactured.[17] The present work focuses on the performance of the DNTT transistors under various measurement conditions in order (a) to obtain a comprehensive appreciation of DNTT transistor stability during intensive operation, (b) to assess long-term stability of DNTT transistors over a period of months and (c) to evaluate the performance of PS-buffered, flash evaporated TPGDA during storage and operation.

2. EXPERIMENTAL SECTION

Bottom gate top contact DNTT transistors were fabricated by vacuum-flash deposition and polymerization of TPGDA (purchased from Sigma-Aldrich) onto 125 μm thick polyethylene naphthalate (PEN) substrates (DuPont Teijin Films), furnished with thermally evaporated Al gate electrodes. The TPGDA layer was 450 nm thick and buffered with a ~40 nm thick polystyrene (purchased from Sigma-Aldrich) film spin-coated from 0.6 wt % toluene solution prior to the evaporation of a ~70 nm thick film of DNTT (synthesized at Manchester University). The capacitance per unit area of the two-layer dielectric was 13 nF/cm^2. The ratio of channel width, W, to channel length, L, of our OTFTs was either 2.4 mm/200 μm or 5 mm/200 μm. Fuller details of the device fabrication procedures can be found in our previous publications.[11,16,17]

Environmental tests were conducted using a small vacuum bell jar. Devices located inside the bell jar could be electrically connected to two source measure units (Keithley model 2400) for measurement of both the transfer characteristics, drain current (I_D) vs gate voltage (V_G), and the gate leakage current (I_G). For most of the tests, the devices were subjected to many cycles of the gate voltage while the drain voltage (V_D) was held at −20 V. For characterization in a vacuum, the chamber was evacuated to a pressure of 10^{-2} mbar. For the dry air measurements, compressed air with humidity <10% at 20 °C was constantly fed into the bell jar. A Lascar EL-USB-1-LCD temperature data logger with LCD screen was placed in the jar to monitor the humidity and temperature during device measurement. A damp air environment was achieved by passing the compressed air through a bubbler filled with water before it entered the chamber. The humidity in the chamber was controlled by the air flow rate and monitored by the in-line humidity sensor. The humidity range was controllable from 10% to 60% at a temperature of 20 °C. A relative humidity of about 55% at 20 °C was used for the damp air measurements.

For the long-term storage test, transistors were placed in (a) a drybox with humidity of 5−10% at 20 °C in the dark, (b) a clean-room atmosphere with relative humidity of 30−60% at 15−25 °C in the dark or (c) uncontrolled ambient air (relative humidity within the range of 20−50% at 15−25 °C) under constant laboratory fluorescent lighting (Osram 18W/840 LUMILUX fluorescent lamp), each for up to 9 months. Transfer measurements were conducted in ambient air either in the bell jar or in a probe station covered by a light-blocking blanket.

3. RESULTS AND DISCUSSION

3.1. Operational Stability. The operational stability of the bottom-gate-top-contact DNTT transistors was investigated by repeatedly measuring their transfer characteristics (up to 50 successive cycles of gate voltage, V_G) in different environments. The transistors were tested in a vacuum, dry air and damp air, both with and without illumination. Assuming that the OTFTs are inert to the nitrogen component of air,[18] the effects of oxygen, moisture and light on the transistors were thus independently identified.

Vacuum in the Dark. The performance of a representative DNTT transistor (with PS-buffered TPGDA dielectric layer) subjected to 10 measurement cycles under a vacuum of 10^{-2} mbar in the dark is presented in Figure 1a. The threshold

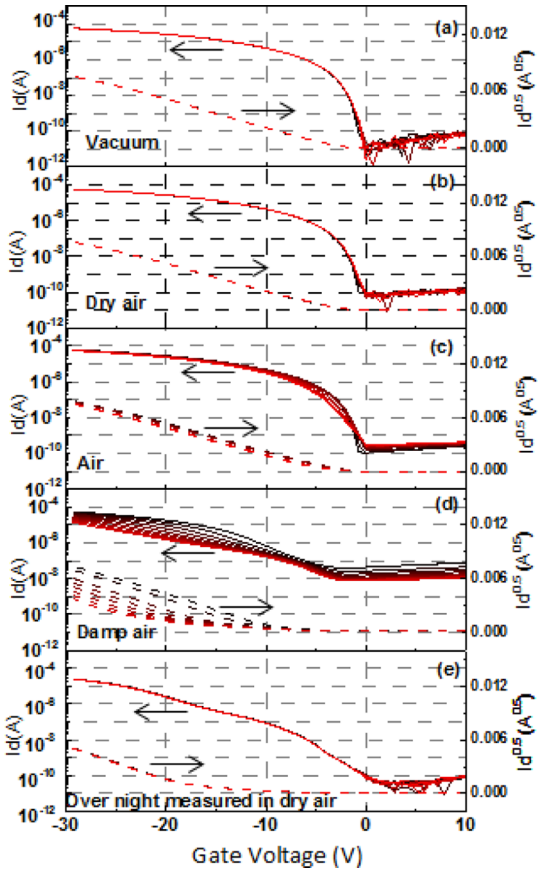

Figure 1. Transfer curves (V_d = −20 V) obtained during 10 repeat gate-voltage sweeps (indicated by solid lines from black to red) of a DNTT transistor with PS-buffered TPGDA dielectric layer measured in (a) a vacuum of 10^{-2} mbar, (b) dry air-relative humidity 5% at 20 °C, (c) clean room air-relative humidity 30% at 20 °C, (d) damp air-relative humidity 55% at of 20 °C and (e) damp air again after placing in a vacuum for 2 h and stored in dry air overnight.

voltage, V_T, turn-on voltage, V_{to}, subthreshold slope, SS, mobility within the saturated region, μ_{sat}, off current, I_{off}, and maximum, I_{on}, are extracted and presented in Table 1. For each cycle, which lasted for about 25 s with no gap between, it is seen that the turn-on voltage, V_{to}, remained constant at 0 V. From the plots of square root of drain current versus gate voltage ($I_D^{0.5}$ vs V_G) shown dotted in Figure 1a, both the threshold voltage, V_T, and mobility, μ, were also seen to remain stable at −2 V and 1 cm^2·V^{-1}·s^{-1}, respectively. The subthreshold swing, SS, improved slightly from 0.6 to 0.4 V/dec over the 10 cycles.

Effect of Oxygen in the Dark. The DNTT device was also stable in dry air of relative humidity ~5% in the dark (Figure 1b, Table 1): a small shift of V_{to} from −0.7 to 0 V and an increase of SS from ~0.6 to ~0.8 V/dec occurred within the first two cycles. Thereafter, no further change was observed. The I_{off} was generally stable at ~10^{-10} A, which is higher than the case in a vacuum measurement, ~10^{-11} A.

Effect of Moisture in the Dark. When devices were measured in uncontrolled air, relative humidity ~30% at 20 °C in the dark, some degradation was noted (Figure 1c, Table 1): the I_{off} increased 3-fold, the on-current decreased by about 10%, V_T shifted from −2 to −4 V and SS increased from 0.6 V/dec to 1.5 V/dec after 10 cycles.

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Table 1. Extracted Parameters of DNTT Transistors in Transfer Cycles Shown in Figures 1, 3 and 5 and Possible Physical Process Involved during Measuring Cycles[a]

		1st cycle/10th cycle						
	condition	V_T (V)	V_{to} (V)	SS	$\mu_{sat\ max}$ (cm^2/(V·s))	I_{off} (A)	I_{on} max (μA)	notes
Figure 1	vac dark	−2/−2	0/0	0.6/0.4	1.0/1.0	~10^{-11}/~10^{-11}	57/57	vac purification
	dry air dark	−2/−2	−0.7/0	0.6/0.8	1.0/1.0	~10^{-10}/~10^{-10}	58/58	oxygen doping[19]
	air dark	−2/−4	−1.0/0	0.6/1.5	1.0/1.0	1×10^{-10}/ 3×10^{-10}	62/56	hole trapping[20]
	damp air dark[b]	−10/−20	−5.0/−2.5	4.1/4.1	1.3/1.6	8×10^{-8}/ 8×10^{-9}	54/13	ionic current[21]/hole trapping[20]
	dry air dark overnight	−16/−16	1.5/1.5	4.0/4.0	1.5/1.5	~10^{-11}/~10^{-11}	25/25	
Figure 3a	vac dark	−2/−2	−1.5/−1.5	0.7/0.6	0.9/0.9	~10^{-11}/~10^{-11}	32/32	vac purification
	vac light	−1.5/−1.5	0	0.8/0.8	1.0/1.0	~10^{-11}/~10^{-11}	35/36	photoexited e/h
	dark again	−2/−2	−1.0/−1.5	0.7/0.5	1.0/1.0	~10^{-11}/~10^{-11}	34/34	vac purification
Figure 3b	dry air dark	2	2.5	0.8	1.2	~10^{-10}/~10^{-10}	44	
	dry air light	4/6	6.0/8.0	0.9/1.0	1.3/1.0	~10^{-10}/~10^{-10}	48/51	O_2 doping[22]/electron trapping[23,24]
Figure 3c	dry air dark (after illum.)	4.5/4.5	6.5/5.5	0.8/0.6	1.1/1.1	~10^{-10}/~10^{-10}	50/49	electron detrapping
	dry air dark (2 h after illum.)	1.5/1.5	3.0/3.0	0.7/0.7	1.2/1.2	~10^{-10}/~10^{-10}	43/44	electron detrapped
Figure 5	dry air light acc.	−1/−1	N/A	1.0/1.0	1.1/1.1	N/A	66/67	
	dry air light acc. and dep.	−1/3	N/A	1.6/2.0	1.1/1.3	N/A	71/85	electron trapping[23,24]/O_2 doping[19,22]
	dry air light acc. Again	0/−0.5	N/A	2.2/1.3	1.3/1.3	N/A	80/74	electron detrapping
	dry air dark acc. and dep.	−1/−1	N/A	1.1/1.1	1.3/1.3	N/A	73/72	

[a]The $\mu_{sat\ max}$ presented are the highest values within the saturation region. [b]Data in this column were extracted from 30th−40th transfer cycles from according transistors, rather than 1st−10th in other cases.

When relative humidity was increased to 55%, changes in device performance were much greater and are clearly seen in Figure 1d. During 4 sets of 10 successive cycles, the transfer curves became distorted and shifted to the left; only the last 10 cycles are presented in Figure 1d and Table 1. V_{to} shifted to about −5 V, suggesting that the flatband voltage had shifted by the corresponding amount as a result of the increase in charge density. This change is consistent with an effective concentration of additional interface trapped holes of ~3.25× 10^{11} cm^{-2} (using the expression $Q = C_iV$, where C_i is area capacitance and V is the shift in V_{to}, this does not take into account any change in C_i with the change in charge density). From the corresponding $I_D^{0.5}$ vs V_G plots, V_T shifted much more to become as negative as −20 V. Because this shift is much larger than that seen for V_{to}, it suggests that moisture has created additional trap states in the DNTT close to the interface with the dielectric. Although the shift in V_T was not recovered even after leaving the device in a vacuum for 2 h initially, then in dry air in the dark overnight, V_{to} returned to a slightly positive value (Figure 1e). It should also be noted that in the devices exposed to moisture, distinct changes occurred in the subthreshold region of the transfer plots that are again indicative of trap states either at the interface or in the DNTT close to in the interface. Interestingly, despite an obvious reduction in the on current, the mobility of damp air samples increased from 1.0 to 1.3 cm^2/(V·s), then reached 1.6 cm^2/(V·s) after 10 cycles and remained at 1.5 cm^2/(V·s) even after recovery overnight in dry air.

Given the polar nature of TPGDA[11] arising from the ester moieties in its molecular structure coupled with the thinness of the PS layer (40 nm), it is likely that atmospheric moisture can diffuse into the dielectric and interact with TPGDA giving rise to hole trapping states that cause the shift in V_{to}. It has also been reported that the polar nature of water induces donor-like traps either at grain boundaries[25−27] or within the crystal lattice[28] in pentacene. A similar effect could be occurring in DNTT. These traps will immobilize holes in the accumulation channel (see graphical abstract (left)) causing the shift in V_T and increasing the subthreshold swing. Traps of particular energy, or a narrow distribution of energies,[20] could also lead to the slight dip in the transfer characteristics seen at about −18 V in Figure 1d,e. The increased mobility indicated in Figure 1d,e is possibly due to this dip, which exaggerates the slope of $I_d^{0.5}$ vs V_G locally.

Apart from the formation of traps within the DNTT, there are two other possible ways the drain current may be affected by water. The first, reported by Li,[25] Richards[29] and Park,[18] is that water may diffuse to the interface between the source electrode and semiconductor forming charge carrier traps. A buildup of trapped holes here with time would ultimately lead to the formation of a barrier to the injection of holes from the source into the semiconductor. This, however, is unlikely to be the case here. When the direction of I_d was reversed by reversing V_D, there was no change in the observed current, confirming that injection conditions were the same in both polarities. The second mechanism, offered by Park[18] and Noh[4] proposed that water at the interface between the dielectric and semiconductor layer formed dipoles that reoriented with gate bias, leading to clockwise hysteresis in the transfer plots. In our work, however, such hysteresis was only observed in a very few cases at very high humidity, >65% at 20 °C (Figure 2a). Weak anticlockwise hysteresis, in contrast, was more frequently found in samples measured in damp and uncontrolled air (Figure 2b). Therefore, the phenomenon of suppression of I_d in damp air

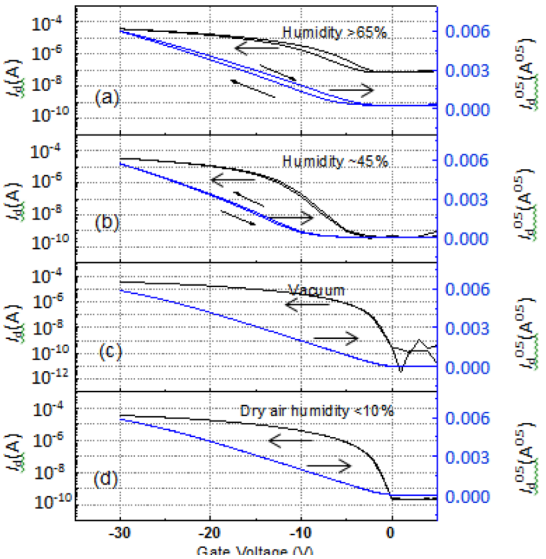

Figure 2. Transfer characteristics of a DNTT transistor fabricated on a PS-buffered TPGDA dielectric measured in the dark at 20 °C in (a) damp air, relative humidity 65−70%, (b) air, relative humidity 45%, (c) vacuum of 10^{-2} mbar, (d) dry air, relative humidity 5−10%.

was probably not, in general, due to the dipole orientation of water molecules at the dielectric surface. Accordingly, donor-like traps are the major cause of the reduction in on-current in the transistor behavior.

The I_{off} in damp air was orders of magnitude greater than in dry air cf. Figure 1b,d and Figure 2a. Upon cycling V_G, this higher value decreased. I_{off} recovered to the original low value when the device was measured in dry air or in a vacuum again. It is likely, therefore, that diffusion of water into the device resulted in an ionic current in the gate dielectric. The decreasing current in the repeat measurements is probably caused by removal of mobile ionic species out of the dielectric by the applied electric field, a process that is well recognized in insulating materials.[21]

Effect of Illumination. A number of publications[20,30−32] have investigated the properties of OTFTs under illumination because of their potential applications as photodetectors. Here the focus is on understanding the role that light may play in the degradation of device properties during operation and storage. Initially, in this section, we report the short-term effects of exposing PS-TPGDA/DNTT transistors to light (Osram 18W/840 LUMILUX fluorescent lamp) when under vacuum, in dry air and in moist air. In section 3.3, longer term changes are investigated.

The response of a typical transistor to illumination when under vacuum is shown in Figure 3a. The transfer characteristics were similar to those measured in the dark except for a minor shift of V_{to} from −1.5 to 0 V. There was 10% increase in I_{on}, more than half of which would have been caused by the flat-band voltage shift of 1.5 V, the remainder from a photocurrent generated in the DNTT. No further changes were observed during repeat measurements. The minor change of the V_{to} as well as the V_T disappeared quickly after the device was placed back into the dark. The carrier mobility and I_{off} were generally stable before and after illumination.

The same illumination experiment was conducted in dry air (Figure 3b) with a similar device, albeit one that had previous measurement history hence the slightly positive V_T = 2.5 V when measured in the dark. In this case, under illumination, V_{to}

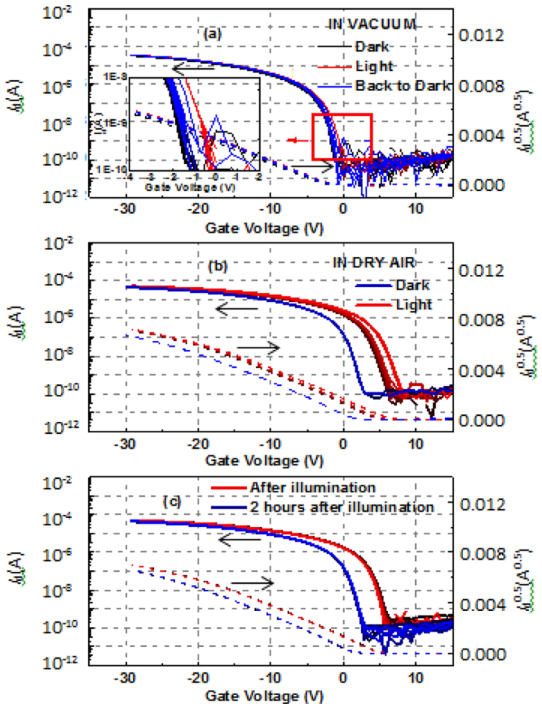

Figure 3. Transfer characteristics of DNTT transistors fabricated on a PS-buffered TPGDA dielectric measured (a) in a vacuum in the dark (black), vacuum under illumination (red), and dark again (blue); (b) in the dark then in the light in dry air (repeat cycles 1st−10th from black to red); (c) the same device measured immediately after it was returned back to dry air in the dark, after recovery under vacuum in the dark for 2 h.

shifted instantly to 6 V and then gradually to 8 V during repeat cycles. The increase in on-current was 15%, unlike the case in illumination in a vacuum, 90% of the I_{on} increase would have been caused by the shift in V_{to}. After illumination was terminated, V_T immediately relaxed back to 4.5 V and remained constant in subsequent cycles (Figure 3c). The V_{to} relaxed back to 6.5 V initially then gradually decreased to 5.5 V after 10 cycles. When placed in the dark under vacuum for 2 h, the transfer curves recovered almost to the state before illumination.

Transistors were also measured under illumination in moist air. As seen in Figures 1d and 4a, significant degradation of the

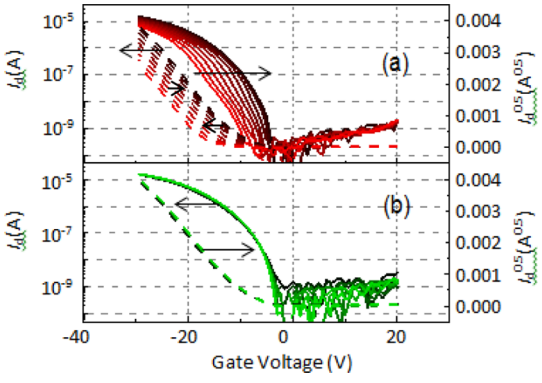

Figure 4. Transfer characteristics of a DNTT transistor measured during repeated gate voltage sweeps (a) in air in the dark (indicated by solid lines from black to red) and (b) in air under laboratory light (indicated by solid lines from black to green).

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transfer characteristics occurred when cycling the gate voltage of a device, in the dark, while exposed to uncontrolled air of relative humidity between 30%−50%, at 20 °C. Interestingly, as shown in Figure 4b, exposure to laboratory fluorescent light for less than 1 min not only erased the degradation but also led to stable operation during repeat cycles in uncontrolled air, so long as the device remained illuminated.

When organic transistors are exposed to light, three types of effects have been reported in the literature, including photoassisted oxidation,[15,16] photoconductive behavior and photovoltage behavior.[33]

Photo-oxidation leads to a decrease in the conjugation length of the semiconductor molecules and, hence, to a significant reduction of charge carrier mobility;[34] however, this was not observed in the DNTT devices, either during the voltage cycling measurements or during the long-term environmental testing discussed in the next section. The molecular design, i.e., substitution of the central carbon ring by a thienothiophene moiety, is effective in preventing photodegradation in DNTT.

The photoconductive behavior, which is due to the photogeneration of mobile electron−hole pairs, would lead to an immediate increase of I_d over the gate voltage sweep range. Figure 3a shows an instant increase of on-current for devices measured under illumination in accord with the photoconductive behavior, and also a quick recovery when the devices are returned to the dark.

A more significant increase of on-current (Figure 3b and Table 1) under light in air was from the photoinduced shift in flat-band voltage, i.e., photovoltage behavior. The photovoltage[32] behavior is attributed to less mobile photogenerated electrons accumulating and becoming trapped at, or near, the semiconductor/dielectric interface. It can lead to large positive shifts in V_{to} and V_T[22−24] and, as a result, lead to higher on-currents. The much greater shift in V_T compared with that in a vacuum (Figure 3a) suggests that such an effect in these devices was associated with the presence of oxygen.

Effect of Oxygen under Illumination. With the assistance of illumination, oxygen doping of the DNTT, either physical or chemical, leads to a higher concentration of acceptor-like trap states for electrons (see graphical abstract (middle)). In the dark, these trap states have little effect, but under illumination, they can be filled by photoexcited electrons, and thus lead to a much stronger, slow response of photovoltage behavior, i.e., shift of V_{to} with repeated measurement under illumination.

It has been proposed[23,24,35] that interface trapping of electrons photogenerated in P3HT-based metal−insulator−semiconductor (MIS) capacitors biased into depletion leads to a shift of the flat band voltage. To check whether this could be the case for the PS-TPGDA/DNTT OTFTs in the present work, a transistor was illuminated while biased only in the accumulation region, i.e., for negative gate voltage only (Figure 5a). Interestingly, the transfer plots were stable over 10 gate-voltage sweeps. This is in contrast to the full-range gate-voltage sweeps applied to the same transistor (Figure 5b) when a significant positive shift of V_T occurred and the SS increased (Table 1). When the gate voltage was cycled again only in the accumulation region, V_T gradually shifted back to less positive V_T (Figure 5c) and the SS recovered. No shift was observed when the device was then measured in the dark (Figure 5d).

We argue, therefore, that interface electron traps created by the presence of oxygen become populated when the device is driven into depletion in the presence of illumination, resulting in the observed positive shift of both V_T and V_{to}.

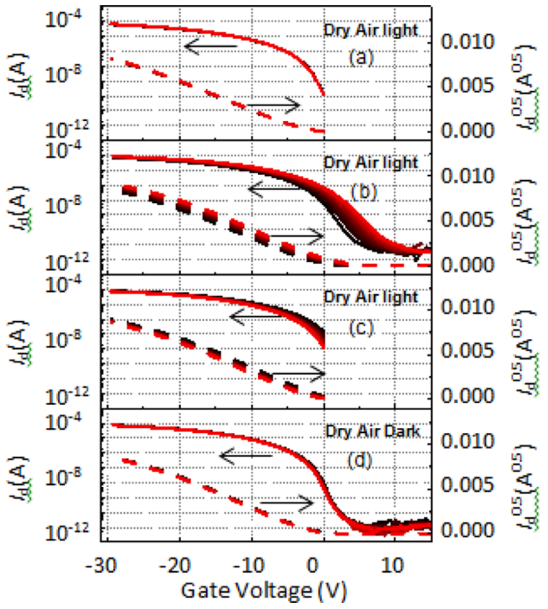

Figure 5. Transfer characteristics of a DNTT transistor fabricated on a PS-buffered TPGDA dielectric layer obtained during successive sweeps of the gate voltage (solid line from black to red) under illumination (a) in the accumulation region only, (b) in both the depletion and the accumulation and (c) in the accumulation again. (d) Successive transfer sweeps covering both the depletion and the accumulation regions but obtained in the dark.

In the case of Figure 4b, transistors illuminated in moist air, the holes trapped on water-related traps were probably neutralized by photogenerated electrons, leading to, essentially, a constant transfer behavior in repeated measurement. It is not clear whether a recombination process was involved[36] or, alternatively, the two types of trapped charges simply matched in number giving a neutral net charge.

3.2. Bias Stress Test. To test the operational stability of our PS-TPGDA/DNTT OTFTs under bias stress, transistors were subjected to constant gate and drain voltages, $V_g = V_d = -20$ V for 144 h in dry air in the dark. Although I_{on} doubled during the bias stress, Figure 6a, there was little sign of degradation in device performance (Figure 6b). The gate leakage current and I_{off} remained very low and V_{to} shifted only moderately from ∼0 to 2.8 V. After several weeks of storage in dry air, the V_{to} recovered its original value. The direction of this shift is to a more positive voltage under negative bias, in contrast to some other reports[2,5,37] that use ceramic dielectric layers. The mobility and SS of the transistor were generally the same before and after the test.

This observed device behavior under long-term bias stress, i.e., (a) increasing on-current with time, (b) constant mobility before and after bias and (c) recoverable transfer characteristics after bias, has not previously been reported for DNTT devices. Similar studies were undertaken by Zschieschang et al.[5] on DNTT transistors fabricated on a SAM treated alumina dielectric layer. In contrast to the increase of I_{on} observed in the present work, they reported that I_{on} started to reduce after 1 hour of bias stress, falling to ∼70% of the original after 24 h. In their devices, SS degraded and the threshold voltage shifted negatively. No recovery was observed after several days of relaxation.

The recovery time of the shift in V_{to} under gate bias in Figure 6b, which could be weeks, was much longer than that observed

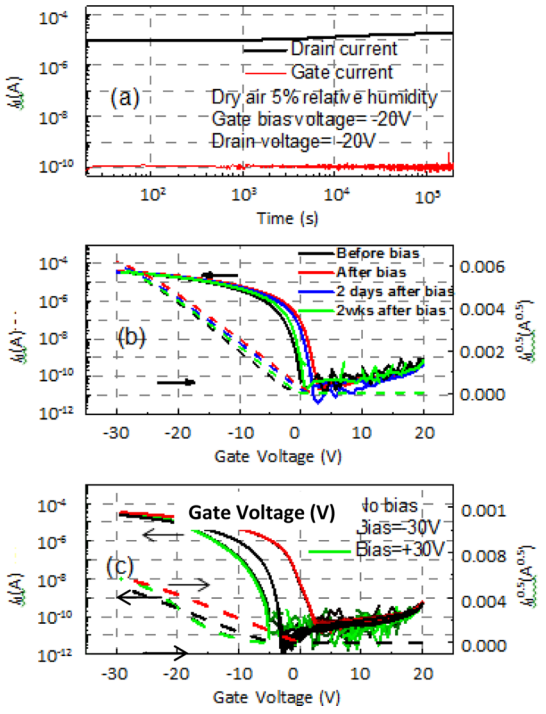

Figure 6. (a) Source-drain current, I_d, and gate leakage current, I_g, of a DNTT transistor subjected to a constant bias, $V_g = V_d = -20$ V, for 144 h in dry air. (b) Transfer curves for the transistor measured before bias, immediately after bias stress and after storing in dry air for two and then 14 days. (c) Transfer characteristics of a DNTT transistor measured before negative bias, after applying $V_g = -30$ V of 12 h and after applying $V_g = 30$ V for 24 h with the drain contact floating.

earlier following the application of successive gate-voltage sweeps, which was only hours (Figure 3), indicating the origin of the shift was different in the two cases.

To identify the cause of the V_{to} shift under bias stress, a gate voltage of −30 V was applied to the device with the source grounded but the drain left floating. In the absence of a channel current, I_d, the probability of hole trapping in the channel area was significantly reduced. As seen in Figure 6c, after 12 h in air, the device transfer characteristic shifted significantly, ∼6 V to more positive potential and the subthreshold swing increased from 0.6 V/dec to 1.2 V/dec, an even more significant change than that observed in the presence of a device current (Figure 6b). Following the period under negative bias stress, a positive gate voltage ($V_g = 30$ V) was applied for 24 h with the drain still kept floating. This opposite stress shifted V_{to} to a more negative potential than seen in the unstressed device. Furthermore, the transfer curve became slightly distorted. The observed polarity of the shifts in V_{to} suggests that the applied gate-source electric field had caused slow polarization of dipolar groups in/on the dielectric layer, and/or charge injection from the gate into dielectric layer. At this stage, it is difficult to differentiate between the two mechanisms. Charge carrier accumulation and trapping processes associated with current flow in the conductive channel, would be expected to lead to shifts in V_{to} of opposite polarity to those seen in Figure 6c and thus are less likely to be the cause for the V_{to} shift in bias test.

3.3. Long-term Environmental Effect. To investigate the long-term environmental stability of DNTT devices, three groups of PS-TPGDA/DNTT transistors fabricated on a polyethylene naphthalate (PEN) substrate were tested over a period of nine months. The details of storage environment can be found in the Experimental Section. The characteristics of all the transistors were measured in the dark. Representative transfer curves obtained during the measurement period are shown in Figure 7. The hole mobilities and subthreshold swings extracted from the transfer curves are presented in Figure 8.

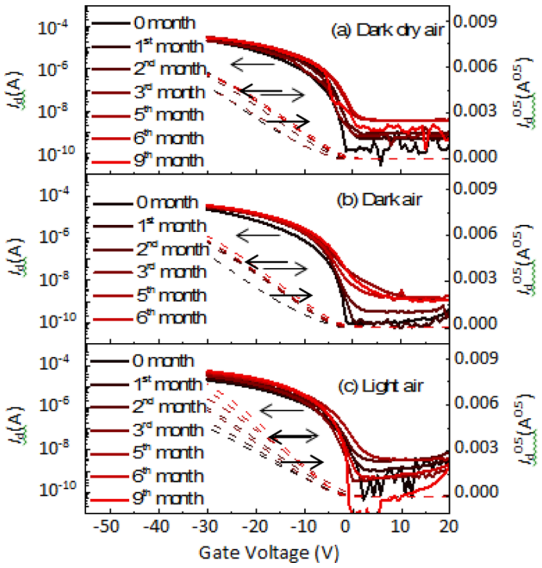

Figure 7. Representative transfer curves of DNTT transistors stored under three different conditions: (a) dry air in the dark, (b) clean-room air in the dark, (c) normal laboratory air and lighting.

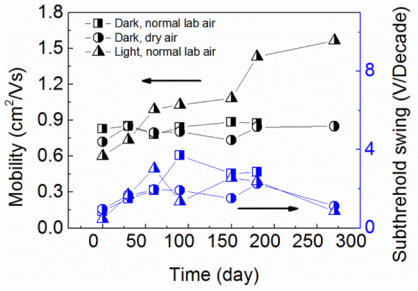

Figure 8. Extracted hole mobilities and subthreshold swings from the transfer characteristics in Figure 7.

The DNTT OTFTs showed exceptionally good environmental stability. When stored in the dark, the mobility of our devices barely shifted over 6 months, irrespective of the environment. For the DNTT device stored in light in air, the mobility gradually increased with storage time, from 0.6 to 1.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$ after 9 months. Such an increase could possibly be due to doping by oxygen molecules diffusing into the semiconductor.[3,22,38−40] This behavior is different to many semiconductors[41,42] that are prone to chemically degrade in oxygen. DNTT is chemically much more stable, so oxidative degradation of the molecule does not occur and, hence, there is no deterioration in the mobility.

The greater SS and the shift of V_T toward higher positive potential for the devices kept in the dark in the cleanroom atmosphere compared with the one stored in dry air suggests that the higher concentration of acceptor-like traps leading to this behavior was associated with water. This somehow conflicts with the results observed during the repeated gate-voltage cycling in Figures 1 and 3, where the traps induced by water suppressed the ability of the device to turn on. In this latter

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case, water appeared to give rise to donor-like traps. A possible explanation could be that gate-voltage cycling was not carried out on the devices kept in long-term storage, so insufficient time was allowed during the testing for significant hole trapping to occur.

Nevertheless, it is clear that substituting the central ring of pentacene with the thienothiophene moiety renders DNTT far less susceptible to oxidative degradation during long-term storage and thus makes it a better candidate for device and circuit applications.

4. CONCLUSION

The electrical stability of bottom-gate, top-contact DNTT OTFTs fabricated on a polystyrene-buffered, flash-evaporated TPGDA dielectric has been investigated under a range different environmental and bias voltage conditions. The results obtained all confirm that the semiconductor/dielectric combination used in our fabrication process leads to devices with exceptionally good stability. In summary, we have shown the following: (a) when subjected to successive gate-voltage sweeps while kept in the dark under vacuum or in dry air, the transfer characteristics of our PS-TPGDA/DNTT transistors were stable. Even when subjected to gate- and drain-voltage stress for 144 h in dry air in the dark, high carrier mobility and high on/off ratios were maintained. Although bias stress and exposure to moisture or illumination all lead to moderate changes in device behavior, these were mostly recoverable by storing the devices in dry air. The hole carrier mobility did not degrade under any of the measurement conditions. (b) Water and oxygen had distinctive effects on the OTFTs. Water not only led to an increased I_{off} but also, more obviously, suppressed/delayed device turn-on by increasing the SS and shifting V_{to} to negative values, thus reducing I_d during operation. The suppression of I_d was attributed to the creation of donor-like hole traps resulting from the presence of water in the semiconductor or at the semiconductor/dielectric interface. In contrast, under illumination in the presence of oxygen, the transfer curve moves toward more positive voltages due to the trapping of photoinduced electrons by acceptor-like traps, when the device is in depletion. The devices were stable when operated only in accumulation mode, i.e., negative gate voltage, under the same condition. (c) In the presence of a gate-source bias with the drain floating, effects related to the acrylic dielectric layer were identified. In particular, over a period of hours, V_{to} shifted by several volts in the opposite direction to the applied bias stress due either to charge injection from the gate into the dielectric or, more likely, by slow polarization of the PS-TPGDA layer. These shifts in V_{to} were recoverable with time or by applying a counter-bias. (d) DNTT transistors could survive storage in dry air, cleanroom air or under normal laboratory air and lighting conditions for more than nine months. Hole mobility was stable over the 9 months as long as the devices were stored in the dark. Interestingly, illumination increased the mobility of DNTT transistors more than 2-fold over the 9 month period, probably due to a light-assisted oxygen doping effect.

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Notes

The authors declare no competing financial interest.

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